

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): ITOU et al.	Atty. Dkt.: 01-470
Serial No.: Unknown	Group Art Unit:
Filed: Concurrently herewith	Examiner:
Title: EEPROM AND EEPROM MANUFACTURING METHOD	

Commissioner for Patents
Arlington, VA 22202

Date: September 12, 2003

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §1.56, the reference(s) listed on the attached Form PTO-1449 is/are being submitted for consideration by the Examiner without any admission that it/they constitute(s) statutory prior art, or without any admission that it/they contain(s) subject matter that anticipates the invention or renders the invention obvious to a person of ordinary skill in the art.

The Examiner is requested to initial the attached PTO Form-1449 and to return a copy of same to the undersigned attorney as proof that the listed reference(s) has/have been considered and made of record.

Respectfully submitted,



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FORM PTO-1449	ATTY. DKT NO.	01-470	SER. NO.
	APPLICANT	ITOUE et al.	
	FILING DATE	September 12, 2003	GROUP

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
		4,477,825 (Corresponding to JP-A-58-115865 which is discussed on page 2 of the spec.)	Oct. 16, 1984	Yaron et al.		
		4,794,562	Dec. 27, 1988	Kato et al.		

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	NAME	CLASS	SUB CLASS	TRANSLATION	YES	NO
		JP-A-59-205763 * (Discussed on page 2 of the spec.)	11/21/84	JAPAN				X (Abstract)		
		JP-A-61-181168 *	8/13/86	JAPAN				X (Abstract)		

* Full English text of the JP Document will be available in machine-translated form from JP (Japanese Patent Office) English language web site at <http://www1.ipdl.jpo.go.jp/PA1/cgi-bin/PA1INDEX>.

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

		Lucero, et al., "A 16 kbit Smart 5 V-Only EEPROM with Redundancy," <u>IEEE Journal of Solid-State Circuits</u> , Vol. SC-18, No. 5, October 1983, pp. 539-544.
EXAMINER		DATE CONSIDERED